800. Gate G_3 has been selected as the signal input **1012**, and gates G_1 and G_2 have been selected as the programming inputs.

An application program access the programmer input **1011** of the programmer **1010** to configure the JFET **800**. The programmer **1010** is coupled to a table memory **1005** that stores data that may include mapped parameters or model coefficients. The programmer **1010** uses the data stored in the table memory **1005** to determine the digitally encoded values that are provided to the digital-to-analog (D/A) converter **1015**.

The D/A converter **1015** receives a digitally encoded voltage value for gates G_1 and G_2 as inputs and applies an analog voltage to gates G_1 and G_2 as outputs.

An application addressing the programmer **1010** provides data that essentially specifies the required characteristics for a single gate JFET. The programmer **1010** uses the data in the table memory **1005** to determine the optimum voltage values to apply to gates G_1 and G_2 in order to achieve the desired response from the JFET **800**. The programmer **1010** may perform a simple table look-up, or may solve an equation or set of equations to determine the optimum voltage values to apply.

FIG. **11** shows a flow diagram for a method **1100** of programming a circuit with a programmable junction field effect transistor such as that shown in FIG. **10**.

In step **1105**, a set of programming voltages is determined. The programming voltages may be an arbitrary sequence of voltages covering the operating range of the device, or they may be voltages selected from voltages provided to other system components.

In step **1110**, a programming input of the device is selected. The programming input may be any of the available gate inputs on the programmable JFET or it may be selected from a predetermined subset of gate inputs.

In step **1115**, a programming voltage is selected from the set of voltages determined in Step **1105**. In step **1120**, the programming voltage is applied. At this point, the programmable JFET is temporarily fixed as a conventional three terminal JFET for succeeding step **1125**.

In step **1125**, the current-voltage (I-V) characteristics of the JFET are determined. This step may be performed over a range of signal input voltages and drain-source voltages as is known in the art. After the I-V characteristics have been determined at the selected programming voltage a check is made in Step **1130** to see if every programming voltage has been evaluated. If the voltage set is not exhausted, steps **1115** through **1125** are repeated. If the set is exhausted step **1135** is performed.

In step **1135**, a parameter table is built from the I-V characteristics determined at each programming voltage. In a simple form, the parameter table may be a collection of the data produced, mapping the I-V characteristics to their associated programming voltages. In an alternative embodiment, the parameter table may also include model coefficients for a general relationship that describes the behavior of the programmable JFET. The model coefficients may be derived from a least-squares or other curve fitting technique.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

The invention claimed is:

1. A programmable circuit comprising:

a programmable junction field effect transistor (JFET) comprising a first gate terminal and a second gate terminal electrically isolated from said first gate terminal, and a source terminal;

a first voltage source coupled to said first gate terminal by a first switch;

a second voltage source coupled to said second gate terminal by a second switch; and

a third switch coupling said first gate terminal to said source terminal, and a fourth switch coupling said second gate terminal to said source terminal;

wherein said programmable circuit is configured to apply said first voltage source and said second voltage source to said programmable JFET independently by, respectively, turning on said first switch and said second switch independently.

2. The programmable circuit of claim **1**, wherein said first switch and said second switch each comprises a transistor.

3. The programmable circuit of claim **1**, wherein said third switch and said fourth switch each comprises a transistor.

4. The programmable circuit of claim **3**, further comprising a first capacitor coupled between said first gate terminal and said source terminal, and a second capacitor coupled between said second gate terminal and said source terminal.

5. The programmable circuit of claim **1**, further comprising a digital-to-analog (D/A) converter coupled to said programmable JFET for providing said first voltage source and said second voltage source.

6. The programmable circuit of claim **5**, further comprising a programmer electrically coupled to said D/A converter.

7. The programmable circuit of claim **6**, wherein the programmer is configured to receive data specifying performance characteristics associated with said programmable JFET and transform said data into first and second voltage values to be applied to said first and second gate terminals, respectively.

8. The programmable circuit of claim **7**, further comprising a memory device electrically coupled to said programmer.

9. The programmable circuit of claim **8**, wherein the programmer is configured to compare said data with data stored in said memory device to determine said first and second voltage values.

10. The programmable circuit of claim **1**, further comprising a first capacitor coupled between said first gate terminal and said source terminal, and a second capacitor coupled between said second gate terminal and said source terminal.

11. The programmable circuit of claim **1**, further comprising:

a third gate terminal electrically isolated from said first gate terminal and said second gate terminal; and

a third voltage source electrically coupled to said third gate terminal.

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